AMENDMENTS TO THE DRAWINGS

As required by the Examiner, submitted herewith is a replacement for sheet 1 of the drawings correctly marked in the page header with the phrase "REPLACEMENT SHEET".

REMARKS

Claims 2 and 4-23 will be pending in the present patent application upon entry of this amendment. Claims 1 and 3 are canceled; claims 18-23 are new; and claims 2, 4-7, 9 and 11-17 are amended.

New claim 18, which replaces canceled claim 1, introduces the following amendments to the as-filed text of claim 1:

> 18. (New) A method for concurrently producing at least a pair of semiconductor structures each including at least one useful layer on a substrate comprising:
>
> providing an initial semiconductor structure that includes ~~a~~ an initial useful layer on ~~a support~~ an initial substrate;
>
> implanting atomic species into the initial useful layer to a controlled mean implantation depth to form a zone of weakness within the useful layer that defines first and second useful layers;
>
> bonding a stiffening substrate to ~~the~~ a front face of the initial structure; and
>
> detaching the first useful layer from the second useful layer along the zone of weakness to ~~obtain~~ produce a pair of semiconductor structures with a first semiconductor structure including the stiffening substrate and the first useful layer and a second semiconductor structure including the initial support substrate and the second useful layer,
>
> wherein the first useful layer and the second useful layer have a thickness such that both the first semiconductor structure and the second semiconductor structure are each individually suitable as an initial semiconductor structure from which a further pair of semiconductor structures can be formed by the steps of implanting, bonding and detaching.

These new amendments to claim 1 as filed particularly point out that either semiconductor structure produced by the steps of providing, implanting, and detaching is individually suitable for further processing by these same steps. All previous amendments to claim 1 as filed are withdrawn in favor of these new amendments. It is thereby intended that the interpretation of this application should not be affected by these prior amendments.

Amended claim 4 together with new claim 21 recite methods in which either the first semiconductor structure produced or the second semiconductor structure produced, respectively, is actually processed. New claims 19 and 20 recite alternatives by which suitable first and second semiconductor structures are produced. New claims 22-23 recite preferred substrates.

OBJECTION TO THE DRAWINGS

Submitted herewith is a replacement for sheet 1 of the drawings corrected as required by the Examiner.

This replacement sheet is being submitted to advance prosecution, but without admission whatsoever by Applicants that all features illustrated in Figs. 1A-C and 2A-C are prior to their application. It is noted that the assertion in the Office Action mailed July 26, 2005 that "only that which is old is illustrated" is not supported by reference to prior art. Applicants reserve rights to petition without prejudice for withdrawal of this requirement.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112

This rejection is now moot because the pending claims do not recite "relatively thick" or "relatively thin", the amendment made in response to the Office Action mailed July 26, 2005 having been withdrawn. However, as suggested in the handwritten correction to the Office Actions, Applicants had indeed intended to recite "only thickness with respect to each other".

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(B)

Claims 1, 3-10, and 12-16 have been rejected under 35 U.S.C. 102(b) as being anticipated by Goesele et al. U.S. Patent No. 6,150,239 ("Goesele"). In response, Applicants respectfully submit that Goesele does not describe, either explicitly or inherently, all of the elements of any pending claim, and therefore that this reference does not anticipate any pending claim.

The present invention describes and claims what, might be called, "chain-reaction" type methods for producing semiconductor structures including a thin semiconductor layer on a substrate: each semiconductor structure produced by these methods can be further processed by the same methods to produce two additional semiconductor structures; each of these two semiconductor structure can then be further processed, and so forth. 1 Figs. 3A-F illustrate the claimed "chain-reaction" process. Fig. 3A illustrates an initial semiconductor structure (5) having a useful semiconductor layer (11) on a substrate (2). A first round of processing according to the pending claims produces two semiconductor structures (51 and 52) having useful semiconductor layers (110 and 120) on substrates (71 and 2). These two structures are illustrated in Fig. 3C. Both of these second round structures in turn have structures similar to initial semiconductor structure (5) and are therefore suitable to be processed as initial structures in a next processing round. When both first round structures are processed in such a second round, four similar second round semiconductor structures are produced (521, 522, 511, and 512), all four of which have useful a semiconductor layer (111, 112, 122, and 121) on a substrate (71, 72, 73, and 2). These four structures are illustrated in Fig. 3F. Figs. 4A-F and 5A-F illustrate alternatives in which the semiconductor structures have additional layers (3 and 8) beneath either one or both, respectively, of the semiconductor surface layers.

The pending claims particularly recite embodiments of the illustrated "chain-reaction" type methods. Specifically, independent claim 18 recites methods producing two semiconductor structures both of which are configured so either can be further processed into two additional semiconductor structures. Dependent claims 4 and 21 recite methods which actually process one or the other of the two semiconductor structures produced by claim 18. Dependent claims 5, 19, 20 recite embodiments of claim 18 further comprising appropriately selecting the thickness of the initial semiconductor layer on the initial semiconductor structure or appropriately selecting the mean implantation depth.

Goesele does not anticipate any pending claim, because this reference does not describe, or even suggest, the "chain-reaction" type method claimed in this application. Instead, Goesele describes a conventional sequential method in which thin layers are removed from a single initial substrate with a thick semiconductor surface layer2 Stated explicitly, a first layer is removed from the initial substrate; then a second layer is removed from the same initial substrate; then a

---

1 This is similar to a uranium chain reaction, in which the fission of one uranium nucleus produces products which can cause the fission of at least two more uranium nuclei, and so forth.

2 See Goesele at col. 4, line 24 to col. 5, line 33.

third layer is removed from the same initial substrate; and so forth. In Goesele, only the initial substrate can be reused.

> In this method the lower portion of the first substrate remains and can be used to produce additional thin layers for subsequent transfer.
>
> . . .
>
> In the method of the present invention the first substrate, from which the Si layer is transferred, can be reused.[3]

Goesele nowhere describes reusing the substrate which receives a thin semiconductor layer (the "second substrate") from the "first substrate". In contrast, pending claim 18 produces two semiconductor structures both of which can individually be used to produce two further semiconductor structures. And pending claims 4 and 21 recite using actually using both initially-produced semiconductor structures.

Further, Goesele does not inherently anticipate any claim. It is of no consequence that one of Goesele's substrates with a transferred layer might be further processed into two further semiconductor structures by the methods of the pending claims. Such an occasional possibility does not inherently anticipate; inherent anticipation requires that every one of these substrates can be so processed.[4] This is certainly not the case, because, *inter alia*, the transferred semiconductor layer may be too thin for further processing. To obviate this requirement, an Office Action cannot simply select pieces of Goesele in order to craft a possible anticipation of the pending claims. This would constitute impermissible hindsight. Neither Goesele, nor the other references relied on, *inter alia,* suggest Applicant's "chain-reaction" type methods.[5] In fact, it is only the present application which describes these methods.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102(B)

Claims 2, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goesele in view of EP 1174926 A1 to Abe ("Abe") and US 2002/0089016 to Joly et al. ("Joly").

---

[3] See Goesele at col. 1, line 21-24; and col. 3, lines 6-7.

[4] See, e.g., M.P.E.P. § 2112 (IV).

[5] See, e.g., M.P.E.P. § 2142 (II).

It is respectfully submitted that neither Abe nor Joly describe or suggest "chain-reaction" type methods. Consequently, all features of dependent claims 2, 11, and 17 are neither described nor suggested by Goesele, Abe and Joly. These claims are therefore not made obvious by these references.

In summary, neither Goesele alone, nor Goesele combined with Abe or Joly, anticipate or make obvious any of the pending claims. These references, *inter alia*, simply do not describe or suggest all features of the pending claims.

CONCLUSION

According all of the claims in the present application are allowable. Reconsideration of the rejections and allowance of the application are respectfully requested.

Respectfully submitted,

Date: April 20, 2005

Allan A. Fanucci (Reg. No. 30,256)
WINSTON & STRAWN LLP
CUSTOMER NO. 28765
(212) 294-3311